SimAcc: A Configurable Simulator for Customized Accelerators on SoCs.

Konstantinos Iordanou, Oscar Palomar, John Mawer, Cosmin Gorgovan, Andy Nisbet and Mikel Luján.

{first}.{last}@manchester.ac.uk

The University of Manchester

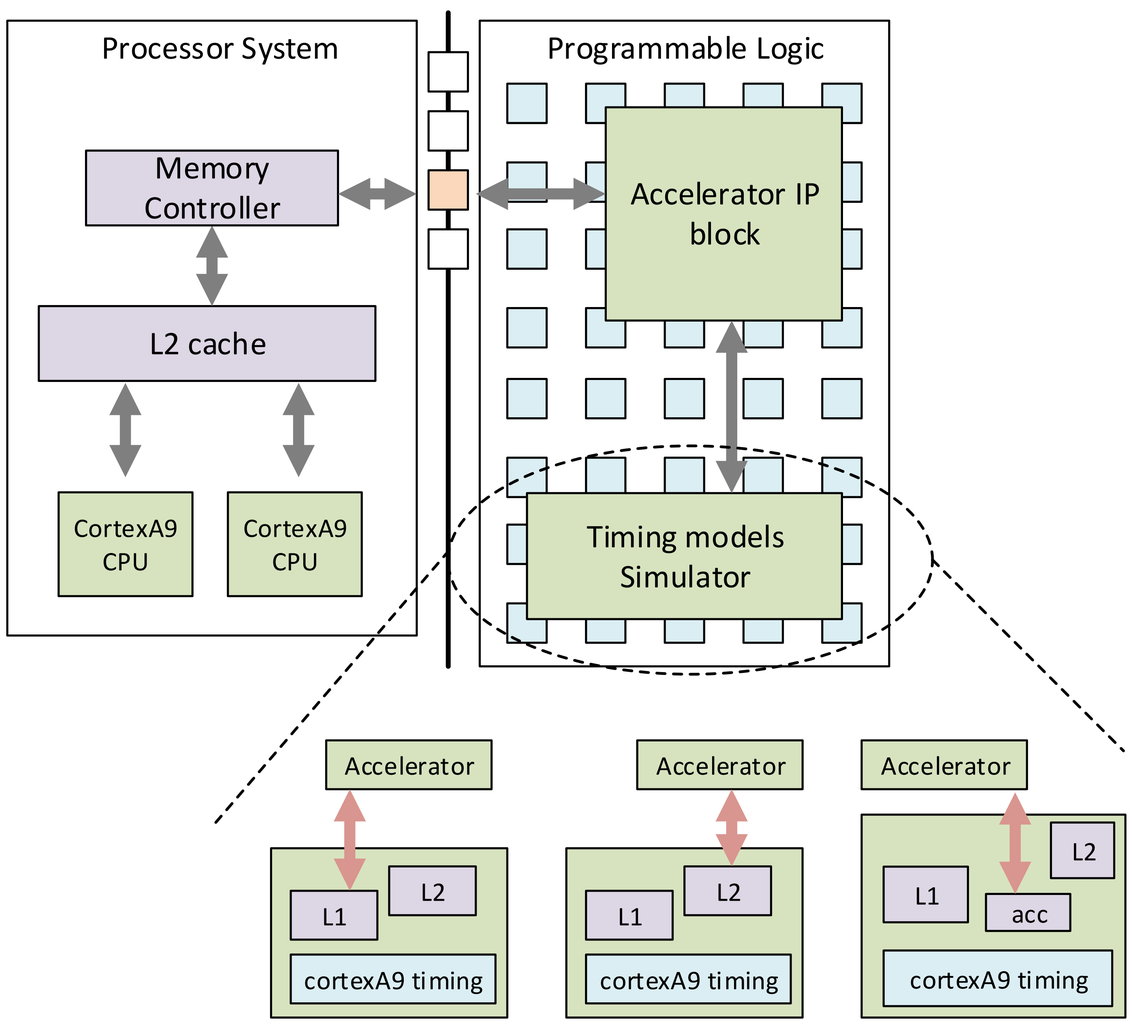
Motivation

- A trend for the System-on-Chips (smartphones,datacenters) is the inclusion of accelerators within the same die for specific applications.
- This trend will lead to heterogeneous systems with many specialised hardware accelerators.

But:
How can we understand the process of generating such hardware accelerators for specific applications?

Simulation of Accelerated Applications

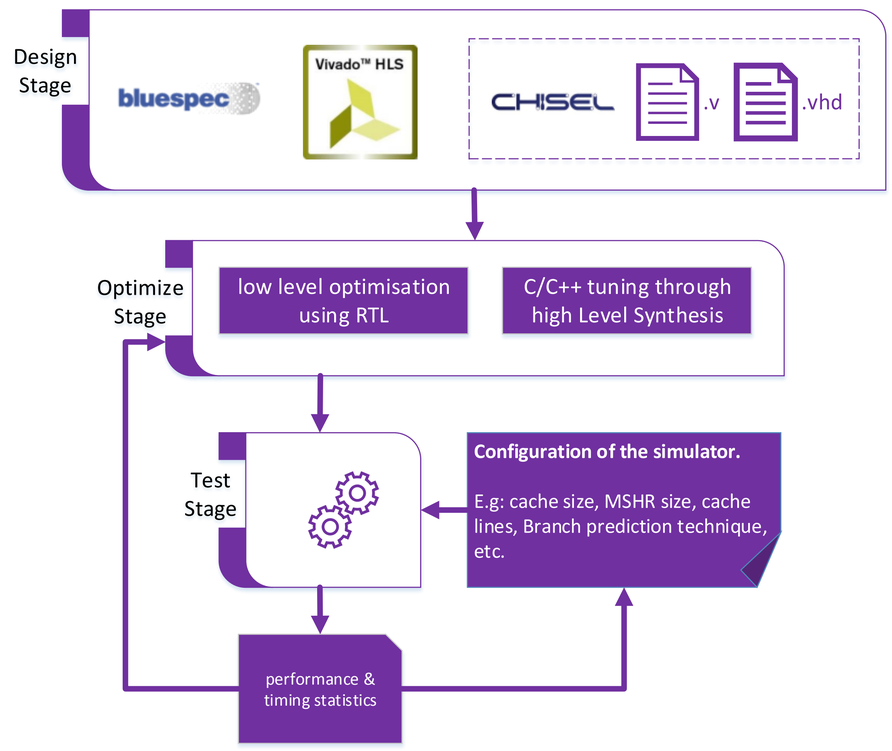
- A methodology for including in the simulation the interaction of processors and accelerators.
- Using unmodified IP blocks, which are wrapped with logic to capture the memory accesses they initiate and simulate them.
- Implementing conventional FPGA-based accelerators, such as image processing filters, and access these from regular applications (Bluespec System Verilog or HLS).
- The proposed system can save a significant part of development time, as end-users can study the timing/performance statistics to identify optimization opportunities, and then re-design their accelerators for test with the same executable.
- SimAcc is composed from three main components:
  - A C++ library and hardware interface standard called MAST. (PS)
  - The dynamic binary modification tool MAMBO. (PS)
  - Hardware timing models for the simulation. (PL)
  - Wrappers to interact with the accelerators. (PL)



Design flow of SimAcc

SimAcc is an infrastructure which allows to test and simultaneously optimize accelerators in an heterogeneous system.

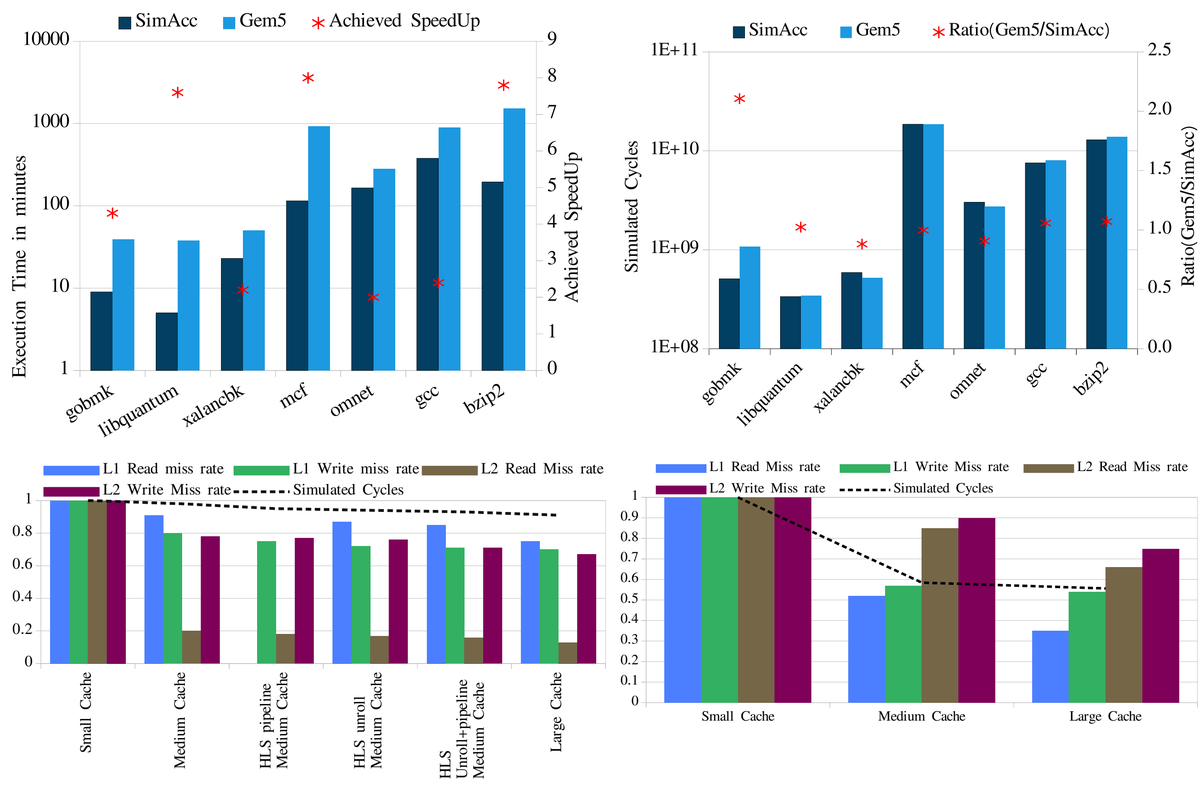
- Produce a hardware configuration to match the desired memory hierarchy and pipeline models parameters.
- Creating the desired models with the Bluespec compiler, the system is ready to be loaded to Vivado.
- Vivado TCL script is used to integrate accelerators and simulator models.



Experimental Evaluation

SimAcc uses:

- A Zynq XC7045 which integrates dual 667MHz Arm Cortex-A9s with substantial FPGA resources.
- Gem5 in system call emulation mode to generate statistics and compare against SimAcc.



References

[1] Cosmin Gorgovan, Amanieu d'Antras, and Mikel Luján. Mambo: A low-overhead dynamic binary modification tool for arm. *ACM Trans. Archit. Code Optim.*, 13(1):14:1–14:26, April 2016.

[2] J. Mawer, O. Palomar, C. Gorgovan, A. Nisbet, W. Toms, and M. Lujan. The potential of dynamic binary modification and cpu-fpga socs for simulation. In *2017 IEEE 25th FCCM Annual International Symposium*, April 2017.

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